Signal Transmission method between stacked chips with resistive-coupling

(Patented in Japan)

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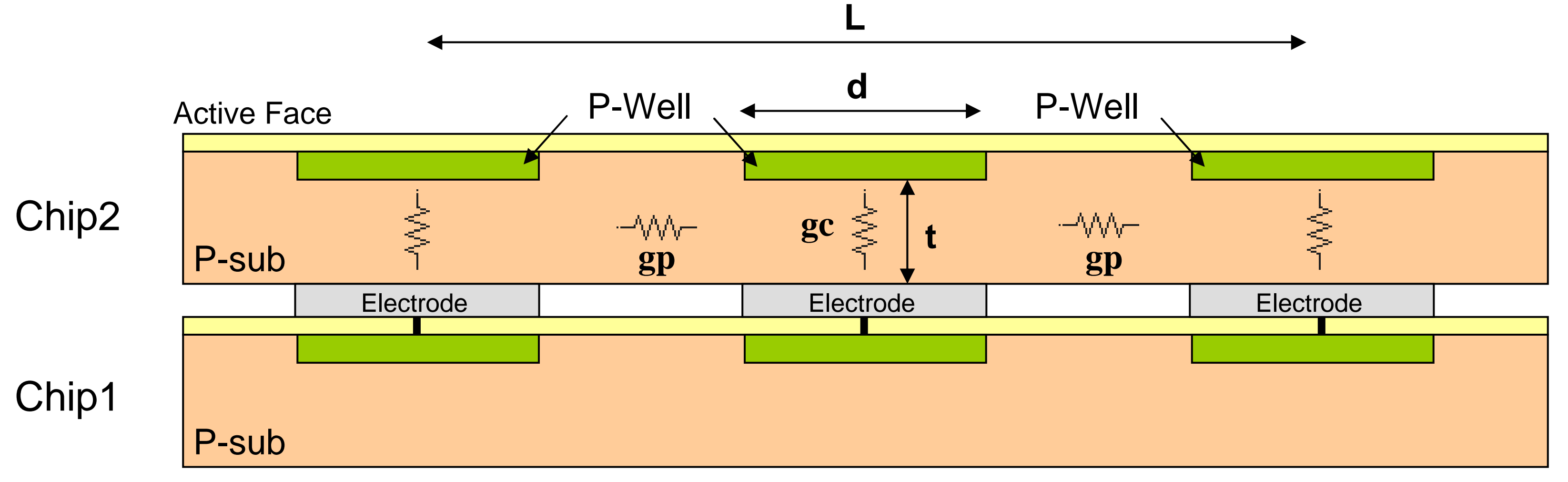
Resistive-Coupling

Signal transmission through the substrate resistance

Coupling from chip1 to chip2 through the backside electrode of chip2 and the substrate resistance of chip1. (VDD/VSS are supplied from wire-bonding or TSV.)



$gc = \pi d^2 / (4 \rho sub \cdot t)$

$2gp = 2\pi t / (\rho sub \cdot \ln(L/d))$

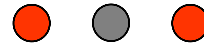
$gc / gp = (d/2t)^2 \cdot \ln(L/d)$

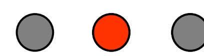
gc,gp: conductance
ρ sub: sub resistivity

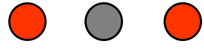
Voltage transfer coefficient
$Av = 1 / \{1+(gc/gp)^{-1}\}$

Av≒0.5 at d=2t, L=3d

Should operate alternately







Comparison Table

	Substrate Resistive-Coupling	Inductive-Coupling	Wire-Bonding
Structure	Active Face, Well, Sub, electrode, Sub	Active Face, Coil, Sub, Sub	Pad, Bonding wire, Sub
Power	◎ ≒1.1mW	× ≒2.8～6.0mW	△ ≒3.0mW
Voltage Transfer coefficient	○ ≒0.5	× <0.1	○ 1.0 (0.5, if terminated)
Frequency Characteristic	◎ ≒2GHz	△ ≒1GHz	△ ≒1GHz
Layout Flexibility	◎	◎	×